Kimia Zamiri Azar

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Research Interest

MAIN INTEREST

VLSI Design, VLSI Testability, Formal Verification, Reconfigurable Architectures, Hardware Security and Trust, IoT Security, Applied Machine Learning.

CURRENT FOCUS OF INTEREST

- **CAD frameworks for System and Security Verification**: Systematic Methods for Verifying and Validating the Security of SoCs, Automation of Security Verification and Validation.
- **Sustainablity and Upgradability for Monitoring and Security Enhancement**: Building Reconfigurable Designs for Security Monitoring on SoCs with Upgradability Possibility.
- **IP/SoC Reverse Engineering Evaluation and Protection**: Security Evaluation of IP Protection Techniques, e.g., Logic Obfuscation and IC Camouflaging.
- **Verification and Assurance Lifecycle in Heterogeneous Integration**: Developing Solutions and Technologies for Security of Chiplet-based Design in System-in-Package (SiP).

Education

Ph.D., Computer Engineering **Aug. 2017 – Aug. 2021**
Department of ECE *George Mason University, USA*
Dissertation: Security Evalution of IP Protection Techniques via Logic Locking **GPA**: 4.00/4.00

M.Sc., Computer Engineering **Aug. 2013 – Aug. 2015**
Department of CE *Shahid Beheshti University, Iran*
Dissertation: Design and HW Implementation of Advanced Binary Division **GPA**: 18.47/20.00

B.Sc., Computer Engineering **Aug. 2009 – Aug. 2013**
Department of ECE *K. N. T. University of Technology, Iran*
Dissertation: Advances in Face Detection Algorithms via Pattern Recognition **GPA**: 17.41/20.00

Professional Experiences

RESEARCH EXPERIENCES

Research Assistant Professor **Sep. 2022 – now**
Department of ECE *University of Florida*

- Conducting Research & Grant Writing, through government/DoD research agencies (DARPA, AFRL, ONR), research consortia (SRC), and national science foundation (NSF).
  - **ONE funded** at DARPA, **ONE funded** at SRC, **THREE submitted** to **NSF SaTC Core/Edu**.
- Mentoring/sub-Advising Graduate Students (Ph.D.) and (M.Sc.).
  - **18 Ph.D.** & **2 M.Sc.** students.
- Technical and Research Sub-advising of Graduate Students.
  - **Accepted Papers at** DATE, ICCAD, ASP-DAC, IEEE Design & Test, GoMACTech, ECTC, ETS.
  - **Three U.S. Patents** and **multiple developed tools and CAD flows**.
- Co-authoring a (Hands-on With Futuristic Roadmap) Book on Hardware Security at **Springer**.

Postdoctoral Research Associate **Sep. 2021 – Sep. 2022**
Department of ECE *University of Florida*

- Technical and Research Lead of of Graduate Students.
  - **5+ papers** at DATE (one best paper nomination), HOST, ASP-DAC, and IEEE TIFS.
  - **Technical Delivery** of DARPA-funded Project and **multiple developed tools and CAD flows**.

- Co-authoring (First-author) of a Book on IP Protection and Reverse Engineering at **Springer**.

Graduate Research Assistant **Aug. 2017 – Aug. 2021**
Department of ECE *George Mason University*

- Research on IP Protection Techniques in VLSI ASIC/FPGA Supply Chain.
  - Investigation/Implementation of (Anti-) Reverse Engineering Methods in IC Supply Chain.
  - **15+ papers** in high prestigious conferences/journals.
    - **Three Best Paper Awards/Nominations**.
    - **One Book Chapter** & **Top Picks in Hardware Security** (on Hardware Reverse Engineering).

- **Technical Lead** of SRC/DARPA Funded Project on Anti-Reverse Engineering Solutions.
  - Implementation of 3D stacked of Obfuscation and Authentication for RE Prevention.
  - Collaborating with Crypto. Eng. Research Group (CERG) Lab at ECE, George Mason University.

Graduate Research Assistant **Aug. 2016 – Aug. 2017**
Department of CE *Sharif University of Technology*

- Research on FPGA-based Accelerator Applications: FPGA-based Network-On-Chips Simulator.
  - **ONE papers Accepted** for publication at **IEEE TC**.

Graduate Research Assistant **Aug. 2014 – Aug. 2015**
Department of CE *Shahid Beheshti University*

TEACHING EXPERIENCES

Lab Instructor and Teaching Assistant **Fall 2018** & **Spring 2019**
Department of ECE *George Mason University*

- ECE445-Computer Organization; ECE448-FPGA Design with VHDL.

Lab Instructor and Teaching Assistant **Fall 2017** & **Spring 2018**
Department of ECE *George Mason University*

- ECE331-Digital System Design; ECE448-FPGA Design with VHDL.

Teaching Assistant **Fall 2014** & **Spring 2015**
Department of CE *Shahid Beheshti University*

- CE4451-Basics of Computer Arithmetic; CE-5452 Advanced Computer Arithmetic.

SUB-ADVISING AND MENTORING EXPERIENCES

Sub-advising and Mentoring as a Research Assistant Professor — **Sep. 2022 – now**
Department of ECE — *University of Florida*

- Muhammad Monir Hossain (Ph.D. Student)
- Hasan Al-Shaikh (Ph.D. Student)
- Mridha Md Mashahedur Rahman (Ph.D. Student)
- Saad Al Haque (Ph.D. Student)
- Rasheed Kibria (Ph.D. Student)
- Md Latifur Rahman (Ph.D. Student)
- Md Habibur Rahman (Ph.D. Student)
- Paul E. Calzada (Ph.D. Student)
- Md Sami Ul Islam Sami (Ph.D. Student)
- Bella Esposito (M.Sc. Student)
- Shams Tarek (Ph.D. Student)
- Nurun N. Mondol (Ph.D. Student)
- Shuvagata Saha (Ph.D. Student)
- Amit Mazumder Shuvo (Ph.D. Student)
- Arash Vafaei (Ph.D. Student)
- Tao Zhang (Ph.D. Student)
- Ahemd Y. Alhurubi (Ph.D. Student)
- Bulbul Ahmed (Ph.D. Student)
- Md Kawser Bepary (Ph.D. Student)

Sub-advising and Mentoring as a Postdoctoral Fellow — **Sep. 2021 – Sep. 2022**
Department of ECE — *University of Florida*

- Muhammad Monir Hossain (Ph.D. Student)
- Hasan Al-Shaikh (Ph.D. Student)
- Mridha Md Mashahedur Rahman (Ph.D. Student)
- Bella Esposito (M.Sc. Student)
- Shams Tarek (Ph.D. Student)
- Nurun N. Mondol (Ph.D. Student)
- Arash Vafaei (Ph.D. Student)

Mentoring as a Ph.D. Student — **Aug. 2017 – Aug. 2020**
Department of ECE — *George Mason University*

- Sanket S Shukla (M.Sc. Student)
- Harshith K. Thirumala (M.Sc. Student)

INDUSTRIAL AND INTERNSHIP EXPERIENCES

Research Intern — **May. 2019 – Aug. 2019**
Hardware Engineer — *Microchip Technologies*

- Research and Development of Hardware Security Solutions into Microchip Technologies.

Research Intern — **May. 2020 – Aug. 2020**
Hardware Engineer — *Microchip Technologies*

- Research and Development of Hardware Security Solutions into Microchip Technologies.

PUBLICATIONS

BOOKS

2024'[B2] Mark Tehranipoor, **Kimia Zamiri Azar**, Hadi Mardani Kamali, Navid Asadizanjani, Fahim Rahman, Farimah Farahmandi, *"Hardware Security: A Look into the Future,"* in Springer, 2023.

2023'[B1] **Kimia Zamiri Azar**, Hadi Mardani Kamali, Farimah Farahmandi, Mark Tehranipoor, *"Understanding Logic Locking,"* in Springer, 2023.

BOOK CHAPTERS

2024'[BC2] Hadi Mardani Kamali, **Kimia Zamiri Azar**, Farimah Farahmandi, Mark Tehranipoor, *"The Prospect of IP Protection via Logic Locking,"* in Future of IP Protection, Springer, 2023.

2022'[BC1] **Kimia Zamiri Azar**, Hadi Mardani Kamali, Avesta Sasan, *"Sequential and Combinational Satisfiability Attacks,"* in Encyclopedia of Cryptography, Security and Privacy (Revisited), Springer, 2022.

PATENTS

2023'[P3] Tao Zhang, Hadi Mardani Kamali, **Kimia Zamiri Azar**, Farimah Farahmandi, Mark Tehranipoor, *"Runtime Security Monitoring of the Hardware against Fault Injection Attacks,"* U.S. Patent, 2023.

2023'[P2] Md Rafid Muttaki, **Kimia Zamiri Azar**, Mark Tehranipoor, Farimah Farahmandi, *"FTC: Fault Injection Attack Detection Solution via Time-to-Digital Converter Sensor,"* U.S. Patent, 2023.

2023'[P1] Rui Guo, M Sazadur Rahman, Fahim Rahman, **Kimia Zamiri Azar**, Hadi Mardani Kamali, Farimah Farahmandi, Mark Tehranipoor, *"UFM Redaction: Automation Fine-grained Redaction Tool for building Universal Protected Hardware,"* U.S. Patent, 2023.

JOURNAL PUBLICATIONS

2023'[J10] Paul E. Calzada, Md Sami Ul Islam Sami, **Kimia Zamiri Azar**, Fahim Rahman, Farimah Farahmandi, Mark Tehranipoor, *"Heterogeneous Integration Supply Chain Integrity through Blockchain and CHSM,"* in ACM Transactions on Design Automation of Electronic Systems (ACM TODAES), 2023.

2023'[J9] Tao Zhang, Latifur Rahman, Hadi Mardani Kamali, **Kimia Zamiri Azar**, Farimah Farahmandi, Mark Tehranipoor, *"SiPGuard: Run-time System-in-Package Security Monitoring via Power Noise Variation,"* in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), 2023.

2023'[J8] Mridha Md Mashahedur Rahman, Shams Tarek, **Kimia Zamiri Azar**, Farimah Farahmandi, Mark Tehranipoor, *"Sustainability of SoC Security Monitoring: From Firmware to embedded FPGA,"* in IEEE Design & Test, 2023.

2023'[J7] **Kimia Zamiri Azar**, Hadi Mardani Kamali, Farimah Farahmandi, Mark Tehranipoor, *"Is Formal Model Checker Scalable for Security Evaluation of Logic Locking? A Semantics-based Design Space Exploration,"* in IEEE Transactions on Information Forensics and Security (IEEE TIFS), 2023.

2022'[J6] Hadi Mardani Kamali, **Kimia Zamiri Azar**, Farimah Farahmandi, Mark Tehranipoor, *"Advances in Logic Locking: Past, Present, and Prospects,"* in IACR Cryptology ePrint Archive, 2022.

2022'[J5] **Kimia Zamiri Azar**, Muhammad Monir Hossain, Arash Vafaei, Hasan Al Shaikh, Nurun N Mondol, Fahim Rahman, Mark Tehranipoor, Farimah Farahmandi, *"Fuzz, Penetration, and AI Testing for SoC Security Verification: Challenges and Solutions,"* in IACR Cryptology ePrint Archive, 2022.

2021'[J4] **Kimia Zamiri Azar**, Hadi Mardani Kamali, Houman Homayoun, Avesta Sasan, *"From Cryptography to Logic Locking: A Survey on the Architecture Evolution of Secure Scan Chains,"* in IEEE Access, 2021.

2021'[J3] **Kimia Zamiri Azar**, Hadi Mardani Kamali, Shervin Roshanisefat, Houman Homayoun, Christos P. Sotiriou, Avesta Sasan, *"Data Flow Obfuscation: A New Paradigm for Obfuscating Circuits,"* in IEEE Transactions on Very Large Scale Integration (VLSI) Systems (IEEE TVLSI), 2021.

2019'[J2] **Kimia Zamiri Azar**, Hadi Mardani Kamali, Houman Homayoun, and Avesta Sasan, *"SMT Attack: Next Generation Attack on Obfuscated Circuits with Capabilities and Performance Beyond The SAT Attacks,"* in IACR Transactions on Cryptographic Hardware and Embedded Systems (IACR TCHES), 2019.

2018'[J1] Hadi Mardani Kamali, **Kimia Zamiri Azar**, and Shaahin Hessabi, *"DuCNoC: A High-Throughput FPGA-Based NoC Simulator Using Dual-Clock Lightweight Router Micro-Architecture,"* in IEEE Transactions on Computers (IEEE TC), 2018.

CONFERENCE PUBLICATIONS

2024'[C26] Nusrat Farzana, Muhammad Monir Hossain, **Kimia Zamiri Azar**, Farimah Farahmandi, Mark Tehranipoor, *"FormalFuzzer: Formal Verification Assisted Fuzz Testing for SoC Vulnerability Detection,"* in Asia and South Pacific Design Automation Conference (ASP-DAC), January, 2024.

2023'[C25] Muhammad Monir Hossain, **Kimia Zamiri Azar**, Farimah Farahmandi, Mark Tehranipoor, *"TaintFuzzer: SoC Security Verification using Taint Inference-enabled Fuzzing,"* in International Conference On Computer Aided Design (ICCAD), November, 2023.

2023'[C24] Hasan Al-Shaikh, Mohammad Bin Monjil, **Kimia Zamiri Azar**, Farimah Farahmandi, Mark Tehranipoor, Fahim Rahman, *"QuardTropy: Detecting and Quantifying Unauthorized Information Leakage in Hardware Designs using g-entropy,"* in IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), October, 2023.

2023'[C23] Mridha Md Mashahedur Rahman, Shams Tarek, **Kimia Zamiri Azar**, Farimah Farahmandi, Mark Tehranipoor, *"EnSAFe: Enabling Sustainable SoC Security Auditing using eFPGA-based Accelerators,"* in IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), October, 2023.

2023'[C22] Muhammad Monir Hossain, **Kimia Zamiri Azar**, Farimah Farahmandi, Mark Tehranipoor, *"EmuFuzzer: Emulation-based Cost Function Guided Fuzzing for SoC Vulnerability Detection,"* in SRC TECHCON, September, 2023.

2023'[C21] M Sazadur Rahman, **Kimia Zamiri Azar**, Farimah Farahmandi, Hadi Mardani Kamali, *"Metrics-to-Methods: Decisive Reverse Engineering Metrics for Resilient Logic Locking,"* in ACM Great Lakes Symposium on VLSI, (GLSVLSI), June, 2023.

2023'[C20] Upoma Das, M Sazadur Rahman, Nalla N Anandakumar, **Kimia Zamiri Azar**, Fahim Rahman, Farimah Farahmandi, Mark Tehranipoor, *"PSC-Watermark: Power Side Channel Based IP Watermarking Using Clock Gates,"* in IEEE European Test Symposium (ETS), May, 2023.

2023'[C19] Muhammad Monir Hossain, Arash Vafaei, **Kimia Zamiri Azar**, Fahim Rahman, Farimah Farahmandi, Mark Tehranipoor, *"SoCFuzzer: SoC Vulnerability Detection using Cost Function enabled Fuzz Testing,"* in Design, Automation and Test in Europe (DATE), April, 2023.
Nominated as Best Paper Candidate.

2023'[C18] Hadi Mardani Kamali **Kimia Zamiri Azar**, Farimah Farahmandi, Mark Tehranipoor, *"SheLL: Shrinking eFPGA Fabrics for Logic Locking,"* in Design, Automation and Test in Europe (DATE), April, 2023.

2023'[C17] Tao Zhang, Hadi Mardani Kamali, **Kimia Zamiri Azar**, Mark Tehranipoor, Farimah Farahmandi, *"FISHI: Fault Injection Detection in Secure Heterogeneous Integration via Power Noise Variation,"* in IEEE 73rd Electronic Components and Technology Conference (ECTC), May, 2023.

2023'[C16] Hasan Al-Shaikh, Mohammad Bin Monjil, **Kimia Zamiri Azar**, Farimah Farahmandi, Mark Tehranipoor, Fahim Rahman *"Quantitative information Flow Analysis of Hardware designs Using Asset Flow Graphs,"* in Government Microcircuit Applications & Critical Technology Conference (GoMACTeh), May, 2023.

2023'[C15] Md Kawser Bepary, Tao Zhang, **Kimia Zamiri Azar**, Fahim Rahman, Farimah Farahmandi, Mark Tehranipoor *"EMSC-GL: Security Assessment and Modeling of electromagnetic Side-channel leakage at Gate-level,"* in Government Microcircuit Applications & Critical Technology Conference (GoMACTeh), May, 2023.

2023'[C14] Hasan Al-Shaikh, Muhammad Monir Hossain, **Kimia Zamiri Azar**, Fahim Rahman, Farimah Farahmandi, *"Cost Function Assisted Fuzz and Penetration Testing for SoC Security Verification,"* in Government Microcircuit Applications & Critical Technology Conference (GoMACTeh), May, 2023.

2023'[C13] Hasan Al-Shaikh, Arash Vafaei, Mridha Md Mashahedur Rahman, **Kimia Zamiri Azar**, Fahim Rahman, Farimah Farahmandi, Mark Tehranipoor, *"SHarPen: SoC Security Verification by Hardware Penetration Test,"* in Asia and South Pacific Design Automation Conference (ASP-DAC), January, 2023.

2022'[C12] **Kimia Zamiri Azar**, Hadi Mardani Kamali, Farimah Farahmandi, Mark Tehranipoor, *"Warm Up before Circuit De-obfuscation? An Exploration through Bounded-Model-Checkers,"* in IEEE International Symposium on Hardware Oriented Security and Trust (HOST), June, 2022.
Recipient of the Best Poster (Work-in-Progress) Award.

2021'[C11] Hadi Mardani Kamali, **Kimia Zamiri Azar**, Houman Homayoun, Avesta Sasan, *"ChaoLock: Yet Another SAT-hard Logic Locking using Chaos Computing,"* in 22nd International Symposium on Quality Electronic Design (ISQED), April, 2021.

2020'[C10] Hadi Mardani Kamali, **Kimia Zamiri Azar**, Shervin Roshanisefat, Ashkan Vakil, Houman Homayou, Avesta Sasan, *"ExTru: A Lightweight, Fast, and Secure Expirable Trust for the Internet of Things,"* in IEEE 14th Circuits and Systems Conference (DCAS), November, 2020.
Recipient of the Best Paper Award.

2020'[C9] **Kimia Zamiri Azar**, Hadi Mardani Kamali, Houman Homayoun, Avesta Sasan, *"NNgSAT: Neural Network guided SAT Attack on Logic Locked Complex Structures,"* in International Conference On Computer Aided Design (ICCAD), November, 2020.

2020'[C8] Hadi Mardani Kamali, **Kimia Zamiri Azar**, Houman Homayoun, Avesta Sasan, *"InterLock: An Intercorrelated Logic and Routing Locking,"* in International Conference On Computer Aided Design (ICCAD), November, 2020.
Nominated as Best Paper Candidate.

2020'[C7] Hadi Mardani Kamali, **Kimia Zamiri Azar**, Houman Homayoun, Avesta Sasan, *"On Designing Secure and Robust Scan Chain for Protecting Obfuscated Logic,"* in Great Lakes Symposium on VLSI (GLSVLSI), July, 2020.

2020'[C6] Hadi Mardani Kamali, **Kimia Zamiri Azar**, Houman Homayoun, Avesta Sasan, *"SCRAMBLE: The State, Connectivity and Routing Augmentation Model for Building Logic Encryption,"* in IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July, 2020.
Nominated as Best Paper Candidate.

2020'[C5] Shervin Roshanisefat, Hadi Mardani Kamali, **Kimia Zamiri Azar**, Houman Homayoun, Avesta Sasan, *"DFSSD: Deep Faults and Shallow State Duality, A Provably Strong Obfuscation Solution for Circuits with Restricted Access to Scan Chain,"* in IEEE VLSI Test Symposium (VTS), April, 2020.

2019'[C4] **Kimia Zamiri Azar**, Farnoud Farahmand, Hadi Mardani Kamali, Shervin Roshanisefat, Houman Homayoun, William Diehl, Kris Gaj, Avesta Sasan, *"COMA: Communication and Obfuscation Management Architecture,"* in International Symposium on Research in Attacks, Intrusions and Defenses (RAID), Beijing, China, September, 2019.

2019'[C3] Hadi Mardani Kamali, **Kimia Zamiri Azar**, Houman Homayoun, and Avesta Sasan, *"Full-Lock: Hard Distributions of SAT instances for Obfuscating Circuits using Fully Configurable Logic and Routing Blocks,"* in Design Automation Conference (DAC), Las Vegas, NV, June, 2019.

2019'[C2] **Kimia Zamiri Azar**, Hadi Mardani Kamali, Houman Homayoun, and Avesta Sasan, *"Threats on Logic Locking: A Decade Later,"* in Great Lakes Symposium on VLSI (GLSVLSI), Tysons Corner, VA, May, 2019.

2018'[C1] Hadi Mardani Kamali, **Kimia Zamiri Azar**, Kris Gaj, Houman Homayoun, and Avesta Sasan, *"LUT-Lock: A Novel LUT-Based Logic Obfuscation for FPGA-Bitstream and ASIC-Hardware Protection,"* in IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Hong Kong, China, August, 2018.

Honors, Distictions, and Awards

2023 **Best Paper Award Nomination** - ONE paper nominated as Best Paper Award Candidate in 2023 Design, Automation and Test in Europe Conference (**DATE Conference 2023**).

2022 **Best Poster Award Recipient** - ONE paper (Work-in-Progress) received the Best Poster Award in 2022 IEEE Symposium on Hardware Oriented Security and Trust (**HOST 2022**).

2020 **Best Paper Award Nomination** - ONE paper nominated as Best Paper Award Candidate in 2020 IEEE/ACM International Conference on Computer-Aided Design (**ICCAD 2020**).

2020 **Best Paper Award Nomination** - ONE paper nominated as Best Paper Award Candidate in 2020 IEEE Computer Society Annual Symposium on VLSI (**ISVLSI 2020**).

2020 **1st Place Competition** - 1st Place (amongst >15 teams) in Cybersecurity Awareness Week (CSAW) Logic Locking Conquest 2020 (**CSAW LLC 2020**).

2020 **Best Paper Award Recipient** - ONE paper received the Best Paper Award in 2020 14th IEEE Circuits and System Conference (**IEEE DCAS 2020**).

2015 **Top Rank (2^{nd}) in Department Graduate Program** - Ranked 2^{nd}, Graduate Program of the CE Department, Shahid Beheshti University, Tehran, Iran.

2013 **Top Rank (3^{rd}) in Department Undergraduate Program** - Ranked 3^{rd}, Undergraduate Program of the CE Department, K. N. Toosi University of Technology, Tehran, Iran.

2013 **Public Graduate (Admission) Grant** - Privileged Admission Grant for Elite (Top Pick) Students, CE Graduate Program, Shahid Beheshti University, Tehran, Iran.

2009 **Top Rank in National University Entrance Exam** - Top 0.5% Among More than 170000 Applicants, National Entrance Exam for Undergraduate Program (Math), Tehran, Iran.

Project Sponsors and Grants

2023 **NSF SaTC: CORE: Medium.** Award Amount: $1,200,000.
Co-PI.

DoD University Research Instrumentation Program (DURIP), Award Amount: $300,000.
Senior Personnel. Co-composing the proposal.

2022-E.2025 **SRC, HWS.3124**, Award Amount: $280,000.
Title: *An Evolutionary AI-based Fuzz Testing for Extensive SoC Security Verification.*
Senior Personnel. Composing the proposal.
Led to **TWO papers** in **ASP-DAC, DATE** and **ONE Best Paper Nomination**.

2020-2021 **Knowledge Design Company**, Award Amount: $510,000.
Title: *Secure Model and Learning protected Hardware Design.*
Co-composing the Proposal.
Led to **2 papers** in **ICCAD**.

2020-2021 **DoD**, Award Amount: $1,250,000.00.
Title: *Corruptive and Hard-to-Break Obfuscation for Semiconductor Devices.*
Co-composing the Proposal.
Led to **5 papers** in **ICCAD, ISVLSI, IEEE TVLSI, IEEE Access, ISQED** and **ONE Best Paper Nomination**.

2018-2021 **AFRL/DARPA**, Award Amount: $1,200,000.00.
Title: *3D Split of Obfuscation, Authentication and Licensing (3D-SOUL).*
Technical/Research Lead (Program + Technical Deliverable Reports).
Led to **12 papers** in **CHES, VTS, RAID, ICCAD, GLSVLSI, ISVLSI, IEEE CAS, IEEE TVSLI, ISQED** and **TWO Best Paper Nominations** and **ONE Best Paper Award**.

2017-2021 **NSF SaTC: STARSS: Small**, Award Amount: $300,000.00
Title: *SaTC: STARSS: Small: IoT Circuit Locking, Obfuscation & Authentication Kernel (CLOAK), A Compilable Architecture for Secure IoT Device Production, Testing, Activation & Operation.*
Technical/Research Lead (Program + Technical Deliverable Reports).
Led to **FIVE papers** in **DAC, ICCAD, RAID, ISVLSI** and **TWO Best Paper Nominations**.

Activities and Services

INVITED TALKS AND PRESENTATIONS

NIST/AFRL/FICS Meeting, Invited Presentation **October 2022**
Title: *Automated and Scalable SoC Security Verification: Challenges and Opportunities*

MEST Center Webinar, Invited Talk **March 2022**
Title: *IP Protection through Logic Locking: What to Expect From the State-of-the-art Techniques*

IEEE CEDA, CADforAssurance, Invited Talk **March 2021**
Title: *The Usage and Applicability of Satisfiability Modulo Theory (SMT) on Logic Locking*

ACM Great Lakes Symposium on VLSI (GLSVLSI), Invited Presentation **May 2019**
Title: *Threats on Logic Locking: A Decade Later.*

TUTORIALS AND TRAINING SESSIONS

IEEE CEDA Trainings, CADforAssurance, Tutorial **March 2021**
Title: *Satisfiability Modulo Theory (SMT) on Logic Locking: A Tutorial*

CAMPUS AND DEPARTMENTAL TALKS/PRESENTATIONS

George Mason University ECE Seminar, Seminar **February 2021**
Title: *Security Evaluation of IP Protection via Logic Locking*

PROGRAM & ORGANIZING COMMITTEE

2024 **IEEE International Symposium on Hardware Oriented Security and Trust (HOST)**.
Publicity Chair, 2024.

2023 **IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS)**.
Technical Program Committee, 2023.

2023 **ACM Great Lakes Symposium on VLSI (GLSVLSI)**.
Technical Program Committee, 2023.

2023 **IEEE International Symposium on Hardware Oriented Security and Trust (HOST)**.
Technical Program Committee, 2023.

2022 **IEEE International Symposium on Hardware Oriented Security and Trust (HOST)**.
Session Chair, 2022.

2022 **CAD for Security Workshop (CAD4Sec)**. AV Chair, 2022.

2019 **IUCRC: Center for Hardware and Embedded System Security and Trust (CHEST)**.
PhD Service Organization, 2019.

TECHNICAL JOURNAL & CONFERENCE REVIEW/REFEREE

2024 Design, Automation, and Test in Europe Conference (**DATE**).
IEEE International Symposium on Hardware Oriented Security and Trust (**HOST**).

2023 IEEE International Symposium on Hardware Oriented Security and Trust (**HOST**).
ACM Great Lakes Symposium on VLSI (**GLSVLSI**).
IEEE 66th International Midwest Symposium on Circuits and Systems (**MWSCAS**).
IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (**IEEE TCAD**).
IEEE Trans. on Very Large Scale Integration (**IEEE TVLSI**).
ACM Journal of Emerging Technologies in Computing Systems (**ACM JETC**)

2022 ACM/IEEE Design Automation Conference (**DAC**).
IEEE International Symposium on Hardware Oriented Security and Trust (**HOST**).
IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (**IEEE TCAD**).
IEEE Trans. on Very Large Scale Integration (**IEEE TVLSI**).
IEEE Journal of Emerging and Selected Topics in Circuits and Systems (**IEEE JETCAS**).

2021 Design, Automation, and Test in Europe Conference (**DATE**).
IEEE Trans. on Very Large Scale Integration (**IEEE TVLSI**).
IEEE Trans. on Computers (**IEEE TC**).

2020 Great Lakes Symposium on VLSI (**GLSVLSI**).
ACM/IEEE Design Automation Conference (**DAC**).
IEEE Computer Society Annual International Symposium on VLSI (**ISVLSI**).
IEEE Trans. on Very Large Scale Integration (**IEEE TVLSI**).

2019 Great Lakes Symposium on VLSI (**GLSVLSI**).
IEEE Computer Society Annual International Symposium on VLSI (**ISVLSI**)
ACM/IEEE Design Automation Conference (**DAC**).